AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1 - 21. (canceled)

22. (currently amended) ~~The integrated circuit of claim 21~~ A signal processing integrated circuit comprising at least one channel and each channel comprising an input coupled to an amplifier, wherein the amplifier processes an input signal coming to the input, each channel further comprising:

an amplifier coupled to said input for processing said input signal and outputting the amplified signal;

a processing circuit for further processing the said amplified signal and outputting a processed signal,

a trigger circuit to produce at least one trigger signal using the said processed signal and output the said trigger signals, and

an output circuit system for outputting said processed signals responsive to said input signals, wherein a polarity switching circuit is connected to said amplifiers.

23. (previously presented) The integrated circuit of claim 22, wherein said polarity switching circuit is externally controlled.

24 - 27. (canceled)

28. (currently amended) ~~The integrated circuit of claim 21~~ A signal processing integrated circuit comprising at least one channel and each channel comprising an input coupled to an amplifier, wherein the amplifier processes an input signal coming to the input, each channel further comprising:

an amplifier coupled to said input for processing said input signal and outputting the amplified signal;

a processing circuit for further processing the said amplified signal and outputting a processed signal,

a trigger circuit to produce at least one trigger signal using the said processed signal and output the said trigger signals, and

an output circuit system for outputting said processed signals responsive to said input signals, further comprising a peak hold or sample and hold circuit coupled to output of at least one of said amplifiers.

29. (currently amended) ~~The integrated circuit of claim 21~~ A signal processing integrated circuit comprising at least one channel and each channel comprising an input coupled to an amplifier, wherein the amplifier processes an input signal coming to the input, each channel further comprising:

an amplifier coupled to said input for processing said input

signal and outputting the amplified signal;

a processing circuit for further processing the said amplified signal and outputting a processed signal,

a trigger circuit to produce at least one trigger signal using the said processed signal and output the said trigger signals, and

an output circuit system for outputting said processed signals responsive to said input signals, further comprising a plurality of comparators connected to said amplifiers.

30. (previously presented) The integrated circuit of claim 29, wherein the said comparators can be at least one of following types; leading edge, zero crossing, constant fraction comparators.

31. (previously presented) The integrated circuit of claim 29, wherein said plurality of comparators enclose at least one pulse height range of the said input signals.

32. (previously presented) The integrated circuit of claim 30, further comprising a circuit coupled to at least one of said plurality of comparators, said circuit producing a fast trigger signal output.

33. (currently amended) The integrated circuit of claim 28, further comprising a circuit ~~to connect~~ connected to an output of

said peak hold or sample and hold circuit is multiplexed to said output circuit system.

34. (previously presented) The integrated circuit of claim 29, wherein an output of at least one of said plurality of comparators initiates a readout cycle of said signal processing integrated circuit.

35 - 38. (canceled)

39. (currently amended) ~~The integrated circuit of claim 21~~ A signal processing integrated circuit comprising at least one channel and each channel comprising an input coupled to an amplifier, wherein the amplifier processes an input signal coming to the input, each channel further comprising:

an amplifier coupled to said input for processing said input signal and outputting the amplified signal;

a processing circuit for further processing the said amplified signal and outputting a processed signal,

a trigger circuit to produce at least one trigger signal using the said processed signal and output the said trigger signals, and

an output circuit system for outputting said processed signals responsive to said input signals, wherein said output circuit system outputs a ~~readout~~ processed signal for one

triggered channel of said plurality of integrated circuit channels and disables all remaining channels of said plurality of integrated circuit channels, wherein a time delay between said readout signal and said disablement of said remaining channels is controlled by an externally supplied signal.

40 - 43. (canceled)

44. (previously presented) The integrated circuit of claim 29, further comprising a first comparator of said plurality of comparators is a low level discriminator, and

wherein at least one of said first comparator produces an output trigger when pulse height of the said processed input signal is larger than a first threshold voltage.

45. (previously presented) The integrated circuit of claim 29, further comprising a second comparator of said plurality of comparators wherein said second comparator is an upper level discriminator, and

wherein said second comparator only produces a signal when pulse height of the said processed input signal is larger than a second threshold voltage.

46. (currently amended) ~~The integrated circuit of claim 21~~ A signal processing integrated circuit comprising at least one

channel and each channel comprising an input coupled to an amplifier, wherein the amplifier processes an input signal coming to the input, each channel further comprising:

an amplifier coupled to said input for processing said input signal and outputting the amplified signal;

a processing circuit for further processing the said amplified signal and outputting a processed signal,

a trigger circuit to produce at least one trigger signal using the said processed signal and output the said trigger signals, and

an output circuit system for outputting said processed signals responsive to said input signals, further comprising ~~circuitry~~ a time difference measurement circuit connected to the output circuit system for measuring the arrival time difference of said input signals between different channels.

47. (canceled)

48. (previously presented) The integrated circuit of claim 29, wherein the plurality of comparators is a single comparator.

49. (previously presented) The integrated circuit of claim 29, wherein at least one of the plurality of comparators is a discriminator.

50. (previously presented) The integrated circuit of claim 29, wherein at least one of the plurality of comparators is a fast comparator.

51 - 52. (canceled)

53. (currently amended) ~~The integrated circuit of claim 21~~ A signal processing integrated circuit comprising at least one channel and each channel comprising an input coupled to an amplifier, wherein the amplifier processes an input signal coming to the input, each channel further comprising:

an amplifier coupled to said input for processing said input signal and outputting the amplified signal;

a processing circuit for further processing the said amplified signal and outputting a processed signal,

a trigger circuit to produce at least one trigger signal using the said processed signal and output the said trigger signals, and

an output circuit system for outputting said processed signals responsive to said input signals, further comprising ~~circuitry for pole zero~~ a pole-zero cancellation circuit connected to the said amplifiers.

54 - 57. (canceled)

58. (previously presented) The integrated circuit of claim 46, further comprising circuitry for measuring time difference of said input signals between different channels by measuring the phase difference of a Sine and Cosine wave simultaneously sent to each channel at the time when the said channel produces a trigger.

59. (new) A signal processing integrated circuit comprising at least one channel and each channel comprising an input, wherein at least one input signal comes to said input, each channel further comprising:

an amplifier coupled to said input processes said input signal and outputs the amplified signal;

a processing circuit further processes said amplified signal and outputs at least one processed signal,

a trigger circuit produces at least one trigger signal using said processed signal and outputs said at least one trigger signal,

a control system configures and controls the functions, and

an output system for outputting said at least one processed signal responsive to said at least one input signal.

60. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one shaping amplifier.

61. (new) The integrated circuit of claim 59, wherein said

processing circuit includes at least one polarity switching circuit.

62. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one pole zero circuit.

63. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one integration circuit.

64. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one differentiating circuit.

65. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one shaping amplifier.

66. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one gain amplifier.

67. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one sample and hold circuit.

67. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one track and hold circuit.

68. (new) The integrated circuit of claim 59, wherein said

processing circuit includes at least one peak hold circuit.

69. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one comparator circuit.

70. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one discriminator circuit.

71. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one digital to analog converter (DAC) circuit.

72. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one analog to digital converter (ADC) circuit.

73. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one baseline restoration circuit.

74. (new) The integrated circuit of claim 59, wherein said processing circuit includes at least one amplifier.

75. (new) The integrated circuit of claim 59, wherein said amplifier is a charge sensitive amplifier.

76. (new) The integrated circuit of claim 59, wherein said amplifier is a transconductance circuit.

77. (new) The integrated circuit of claim 59, wherein said amplifier includes at least one active resistance feedback circuit.

78. (new) The integrated circuit of claim 59, wherein said amplifier includes at least one resistance feedback circuit.

79. (new) The integrated circuit of claim 59, wherein said amplifier includes at least one transistor feedback circuit.

80. (new) The integrated circuit of claim 59, wherein said amplifier includes at least one MOSFET feedback circuit.

81. (new) The integrated circuit of claim 59, wherein said amplifier includes at least one capacitance feedback circuit.

82. (new) The integrated circuit of claim 59, wherein said amplifier includes at least one gain selection.

83. (new) The integrated circuit of claim 59, wherein said amplifier includes at least one offset adjustment circuit.

84. (new) The integrated circuit of claim 59, wherein said amplifier includes a self reset circuit.

85. (new) The integrated circuit of claim 59, wherein said amplifier includes at least one input capacitance optimization.

86. (new) The integrated circuit of claim 59, wherein said amplifier includes at least one shaping circuit.

87. (new) The integrated circuit of claim 59, wherein said trigger circuit includes at least one comparator.

88. (new) The integrated circuit of claim 59, wherein said trigger circuit includes at least one discriminator.

89. (new) The integrated circuit of claim 59, wherein said trigger circuit includes at least one differentiator.

90. (new) The integrated circuit of claim 59, wherein said trigger circuit includes at least one integrator.

91. (new) The integrated circuit of claim 59, wherein said trigger circuit produces at least one fast trigger signal for accurate timing.

92. (new) The integrated circuit of claim 59, wherein said output system outputs said at least one processed signal if the processed signal produces a trigger signal.